# Lab 11 Sequence Detector

**Objective**

The objective of this lab is to design a synchronous sequence detector that detects a bit-pattern “110”.

We want to design a circuit which detects (110) sequences in a string of bits coming through an input line (i.e., the input is a serial bit stream). Once the (110) sequence is detected, output becomes (1), otherwise it stays as (0). A sample input and output bit streams (sequence) are given below. First bit coming to the input is the one shown on the far left.

Example Input bit stream: x= 0100110010100010110100

time

Example Output bit stream: y= 0000010000000000010000

The diagram of the sequence detector is shown below. Beside the clock, input x and output y, it has a reset input to force the detector into the initial state (“00”). The circuit also output the present state.

1

1

y

reset

Sequence Detector

state

x

1

2

clock

**Lab Procedure**

1. Derive the State Diagram for a **Moore** “110” sequence detector:

Shape

Description automatically generated

1. Write a Verilog code to implement the sequence detector in behavioral level

module sequence\_detector(clock, reset, x, y, state);

*// input*

     input clock, reset, x;

*// output*

     output y;

     output [1:0] state; *// state is 2-bit*

     reg [1:0] state;

   always @( posedge clock, posedge reset ) *// state machine*

       if (reset)

         state <= 2'b00; *// reset state*

   else

       case (state)

         2'b00: if(x)state <= 2'b01;   else state <= 2'b00;

         2'b01: if(x)state <= 2'b10;   else state <= 2'b00;

         2'b10: if(x)state <= 2'b10;   else state <= 2'b11;

         2'b11: if(x)state <= 2'b01;   else state <= 2'b00;

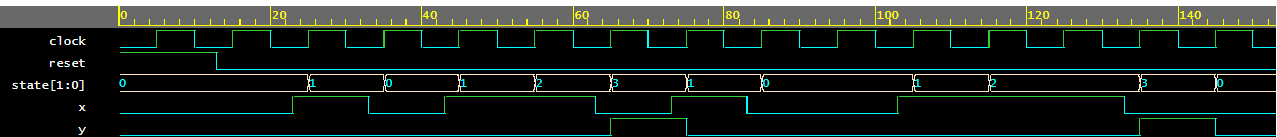
       endcase

*// output y at state “11”*

  assign  y = state[1] & state[0]; *// state[1] is the MSB*

endmodule

1. On the EDAplayground.com, create a Verilog testbench to test your sequence detector and perform the simulation to check if the results are correct. You should generate the input stimuli (x, reset) as shown in the below timing diagram and produce the corresponding outputs (y, state).



module test;

  reg clock, x, reset;

  wire y;

  wire [1:0] state;

*// instantiate the uut*

  sequence\_detector uut(clock, reset, x, y, state);

*//generating the clock signal*

  initial

    begin

      clock = 0; *// clock starts low*

      forever #5 clock = ~clock; *// toggle clock*

      #200 $finish; *// stop simulation after 200 clock cycles*

    end

  initial

    begin

      $dumpfile("dump.vcd"); $dumpvars(1,test);

*// monitor the state, x, and y signals*

      $monitor("state = %b x = %b y = %b ", state,x,y);

*// Initalize inputs*

      x = 0; reset = 1;

      #13  reset = 0; *// hold reset low for 13 clock cycles*

      #10   x = 1; *// set x high for 10 clock cycles*

      #10   x = 0; *// set x low for 10 clock cycles*

      #10   x = 1;

      #10   x = 1;

      #10   x = 0;

      #10   x = 1;

      #10   x = 0;

      #10   x = 0;

      #10   x = 1;

      #10   x = 1;

      #10   x = 1;

      #10   x = 0;

      #10   x = 0;

      #10 $finish;  *// stop simulation after 200 clock cycles*

    end

endmodule

Graphical user interface

Description automatically generated

**Homework**: design a FSM machine for detecting sequence “001” by deriving a state diagram and implement it using Verilog.

**Submission Instructions:**

Lab work submission

1. Take a screenshot of your wavefroms.
2. Add the following information as comments to the beginning of your code. Make sure to click the “Save” button to save your project, then take a screenshot of your code.

// Author: Name

// Lab 11: put the title here

// Link to your project

1. Copy the link of your design from the address bar of the browser.
2. On the Blackboard, click on Lab 11. Attach the screenshot from the first two steps and paste the link from Step 3 into the Comments area, then click the “Submit” button.

Lab report submission

1. Lab report is needed for this lab. Please follow the guidelines and sample report on the Blackboard when you are writing your lab reports. Click on **Lab 11 Report Submission** to submit your report. It is due one week after the lab is done.